

SPECIFICATION

Device Name : IGBT - IPM

Type Name : 7MBP50RU2A120

Spec. No. : MS6M01051

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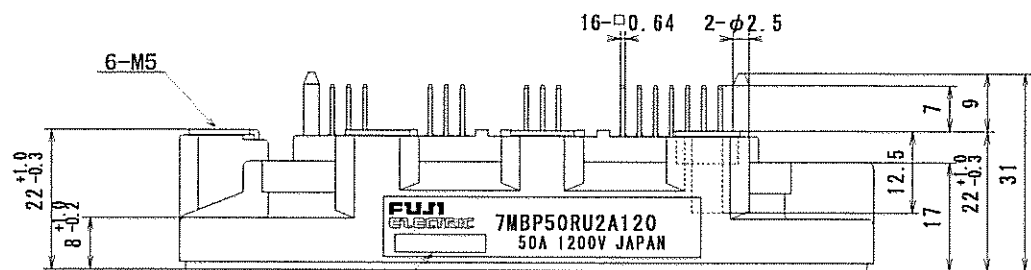
	DATE	NAME	APPROVED	Fuji Electric Device Technology Co., Ltd.			
DRAWN	Jan. - 5 - '06	<i>N. Matsuda</i>		DWG. NO.	MS6M01051	1 / 23	
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Revised Records

Date	Classification	Ind.	Content	Applied date	Drawn	Checked	Checked	Approved
Jan. 5-'06	Enactment	-	-	Issued date	N. Matsuda	M. Matsuda	K. Yamada	T. M. J. S. O. C.

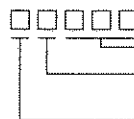
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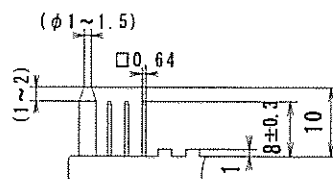
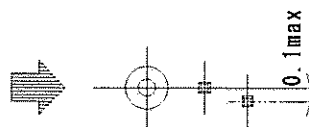
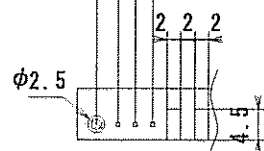
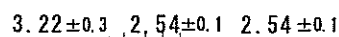
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Lot No.

Indication of Lot No.



Ordered No. in monthly
Manufactured month
(Jan. ~Sep. :1~9, Oct. :0, Nov. :N, Dec. :D)
Last digit of manufactured year



Details of control terminals

Dimensions in mm

DWG.NO.

$$\frac{3}{23}$$

H04-004-03a

2. Pin Descriptions

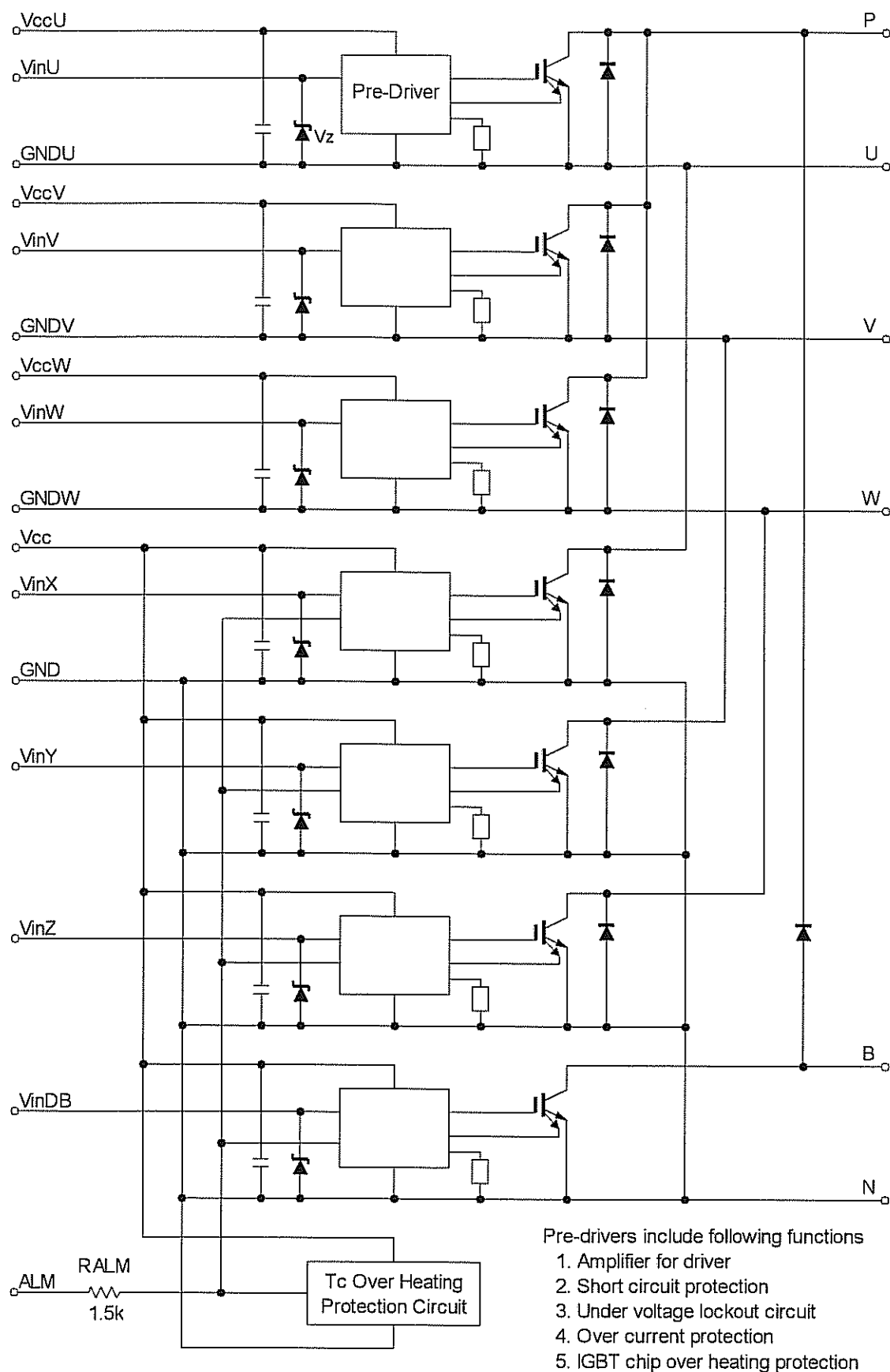
2.1 Main circuit

Symbol	Description
U	Output (U).
V	Output (V).
W	Output (W).
N	Negative input supply voltage.
P	Positive input supply voltage.
B	Collector terminal of Brake IGBT.

2.2 Control circuit

No	Symbol	Description
①	GNDU	High side ground (U).
②	VinU	Logic input for IGBT gate drive (U).
③	VccU	High side supply voltage (U).
④	GNDV	High side ground (V).
⑤	VinV	Logic input for IGBT gate drive (V).
⑥	VccV	High side supply voltage (V).
⑦	GNDW	High side ground (W).
⑧	VinW	Logic input for IGBT gate drive (W).
⑨	VccW	High side supply voltage (W).
⑩	GND	Low side ground.
⑪	Vcc	Low side supply voltage.
⑫	VinDB	Logic input for Brake IGBT gate drive.
⑬	VinX	Logic input for IGBT gate drive (X).
⑭	VinY	Logic input for IGBT gate drive (Y).
⑮	VinZ	Logic input for IGBT gate drive (Z).
⑯	ALM	Low side alarm signal output.

3. Block Diagram



4. Absolute Maximum Ratings

Tc=25°C unless otherwise specified.

Items		Symbol	Min.	Max.	Units	
Bus Voltage (between terminal P and N)		DC	V _{DC}	0	900	V
		Surge	V _{DC(surge)}	0	1000	V
		Short operating	V _{sc}	400	800	V
Collector-Emitter Voltage *1		V _{ces}	0	1200	V	
Inverter	Collector Current	DC	I _c	-	50	A
		1ms	I _{cp}	-	100	A
		Duty=100% *2	-I _c	-	50	A
	Collector Power Dissipation	One transistor *3	P _c	-	300	W
Brake	Collector Current	DC	I _c	-	25	A
		1ms	I _{cp}	-	50	A
	Forward Current of Diode		I _F	-	25	A
	Collector Power Dissipation	One transistor *3	P _c	-	172	W
Supply Voltage of Pre-Driver *4		V _{cc}	-0.5	20	V	
Input Signal Voltage *5		V _{in}	-0.5	V _{cc} +0.5	V	
Input Signal Current		I _{in}	-	3	mA	
Alarm Signal Voltage *6		V _{ALM}	-0.5	V _{cc}	V	
Alarm Signal Current *7		I _{ALM}	-	20	mA	
Junction Temperature		T _j	-	150	°C	
Operating Case Temperature		T _{opr}	-20	100	°C	
Storage Temperature		T _{stg}	-40	125	°C	
Isolating Voltage *8		V _{iso}	-	AC2500	V _{rms}	
Screw Torque		Terminal (M5)	-	-	3.5	Nm
		Mounting (M5)				

Notes

- *1: V_{ces} shall be applied to the input voltage between terminal P and U or V or W or DB, N and U or V or W or DB
- *2: Duty=125°C/R_{th(j-c)}D/(I_c×V_F MAX) × 100
- *3: P_c=125°C/R_{th(j-c)}Q=300W (Inverter)
P_c=125°C/R_{th(j-c)}Q=172W (Brake)
- *4: V_{cc} shall be applied to the input voltage between terminal No.3 and 1, 6 and 4, 9 and 7, 11 and 10.
- *5: V_{in} shall be applied to the input voltage between terminal No.2 and 1, 5 and 4, 8 and 7, 12~15 and 10.
- *6: VALM shall be applied to the voltage between terminal No.16 and 10.
- *7: I_{ALM} shall be applied to the input current to terminal No.16.
- *8: Terminal to base, 50/60Hz sine wave 1min.

5. Electrical Characteristics

$T_j=25^{\circ}\text{C}$, $V_{cc}=15\text{V}$ unless otherwise specified.

5.1 Main circuit

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Inverter	Collector Current at off signal input	I_{CES} $V_{ce}=1200\text{V}$ V_{in} terminal open.	-	-	1.0	mA
	Collector-Emitter saturation voltage	$V_{CE(sat)}$ $I_c=50\text{A}$ Fig.4	Terminal	-	1.9	V
			Chip	-	1.8	V
	Forward voltage of FWD	V_F $-I_c=50\text{A}$ Fig.5	Terminal	-	2.2	V
			Chip	-	2.1	V
Brake	Collector Current at off signal input	I_{CES} $V_{ce}=1200\text{V}$ V_{in} terminal open.	-	-	1.0	mA
	Collector-Emitter saturation voltage	$V_{CE(sat)}$ $I_c=25\text{A}$ Fig.4	Terminal	-	1.9	V
			Chip	-	-	V
	Forward voltage of FWD	V_F $-I_c=25\text{A}$ Fig.5	Terminal	-	2.1	V
			Chip	-	-	V
Turn-on time	t_{on}	$V_{DC}=600\text{V}$, $T_j=125^{\circ}\text{C}$	1.2	1.8	-	μs
Turn-off time	t_{off}	$I_c=50\text{A}$ Fig.1,6	-	2.6	3.6	μs
Reverse recovery time	t_{rr}	$V_{DC}=600\text{V}$ $I_F=50\text{A}$ Fig.1,6	-	-	0.3	μs

5.2 Control circuit

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply current of P-side pre-driver (per one unit)	I_{ccp}	Switching Frequency = 0-15kHz	-	-	18	mA
Supply current of N-side pre-driver	I_{ccn}	$T_c=-20\sim 100^{\circ}\text{C}$ Fig.7	-	-	72	mA
Input signal threshold voltage	$V_{inH(on)}$	V_{in-GND} ON	1.00	1.35	1.70	V
	$V_{inH(off)}$	V_{in-GND} OFF	1.25	1.60	1.95	V
Input Zener Voltage	V_Z	$R_{in}=20\text{k}\Omega$	-	8.0	-	V
Alarm Signal Hold Time	t_{ALM}	$ALM-GND$ $T_c=-20^{\circ}\text{C}$	1.1	-	-	ms
		$T_c=25^{\circ}\text{C}$	-	2.0	-	ms
		$T_c=125^{\circ}\text{C}$ Fig.2	-	-	4.0	ms
Resistor for current limit	R_{ALM}		1425	1500	1575	Ω

5.3 Protection Circuit (Vcc=15V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Over Current	Inverter	Tj=125°C Fig.3	75	-	-	A
Protection Level	Brake		38	-	-	A
Over Current Protection Delay time	tdoc	Tj=125°C	-	5	-	μs
SC Protection Delay time	tsc	Tj=125°C Fig.8	-	-	8	μs
IGBT Chips Over Heating	TjOH	Surface of	150	-	-	°C
Protection Temperature Level		IGBT Chips				
Over Heating Protection Hysteresis	TjH		-	20	-	°C
Case Over Heating	TcOH	VDC=0V, Ic=0A	110	-	125	°C
Protection Temperature Level		Case Temperature				
Over Heating Protection Hysteresis	TcH		-	20	-	°C
Under Voltage Protection Level	VUV		11.0	-	12.5	V
Under Voltage Protection Hysteresis	VH		0.2	0.5	-	V

6. Thermal Characteristics (Tc = 25°C)

Item			Symbol	Min.	Typ.	Max.	Units
Junction to Case Thermal Resistance *9	Inverter	IGBT	Rth(j-c)Q	-	-	0.42	°C/W
		FWD	Rth(j-c)D	-	-	0.99	°C/W
	Brake	IGBT	Rth(j-c)Q	-	-	0.73	°C/W
		FWD	Rth(j-c)D	-	-	2.05	°C/W
Case to Fin Thermal Resistance with Compound			Rth(c-f)	-	0.05	-	°C/W

*9: For 1device , Case is under the device

7. Noise Immunity (Vdc=300V, Vcc=15V, Test Circuit Fig 9.)

Item	Conditions	Min.	Typ.	Max.	Units
Common mode	Pulse width 1us,polarity ±, 10 minuets	±2.0	-	-	kV
rectangular noise	Judge: no over-current, no miss operating				
Common mode	Rise time 1.2us,Fall time 50usinterval 20s,10 times	±5.0	-	-	kV
lightning surge	Judge: no over-current, no miss operating				

8. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units
DC Bus Voltage	VDC	-	-	800	V
Power Supply Voltage of Pre-Driver	Vcc	13.5	15.0	16.5	V
Screw Torque (M5)	-	2.5	-	3.0	Nm

9. Weight

Item	Symbol	Min.	Typ.	Max.	Units
Weight	Wt	-	450	-	g

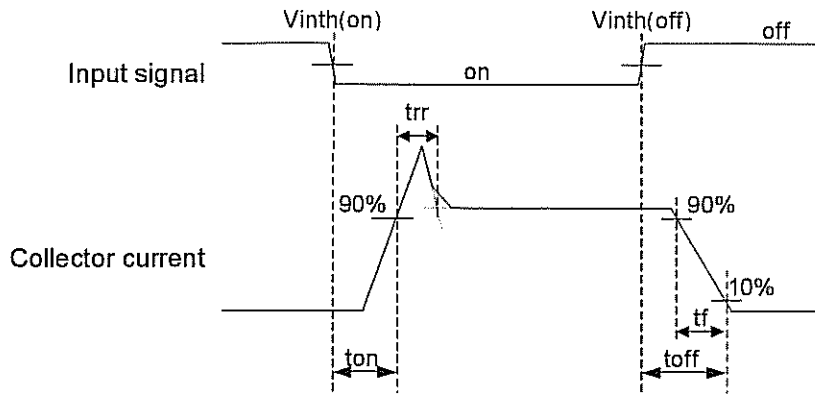


Figure1. Switching Time Waveform Definitions.

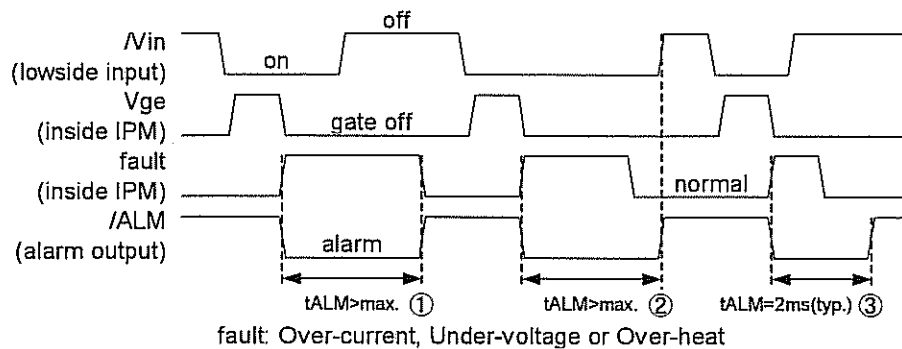


Figure2. Input/Output Timing Diagram.

Necessary conditions for alarm reset (refer to ① to ③ in figure2.)

- ① This represents the case when a failure-causing Fault lasts for a period more than t_{ALM} . The alarm resets when the input V_{in} is OFF and the Fault has disappeared.
- ② This represents the case when the ON condition of the input V_{in} lasts for a period more than t_{ALM} . The alarm resets when the V_{in} turns OFF under no Fault conditions.
- ③ This represents the case when the Fault disappears and the V_{in} turns OFF within t_{ALM} . The alarm resets after lasting for a period of the specified time t_{ALM} .

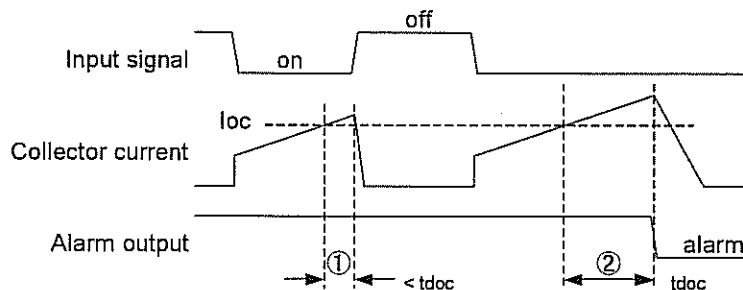


Figure3. Over-current Protection Timing Diagram.

- Period ①: When a collector current over the OC level flows and the OFF command is input within a period less than the trip delay time t_{doc} , the current is hard-interrupted and no alarm is output.
- Period ②: When a collector current over the OC level flows for a period more than the trip delay time t_{doc} , the current is soft-interrupted. If this is detected at the lower arm IGBTs, an alarm is output.

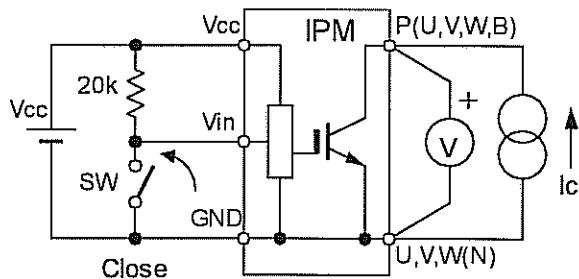


Figure4. Vce(sat) Test Circuit (Terminal)

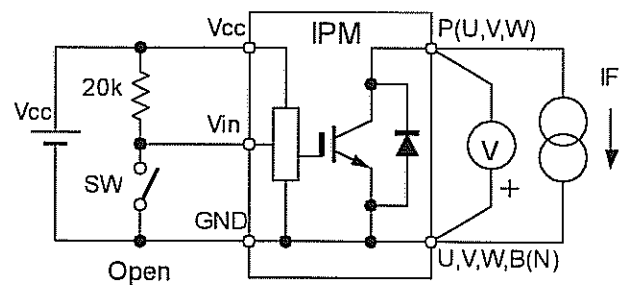


Figure5. VF Test Circuit (Terminal)

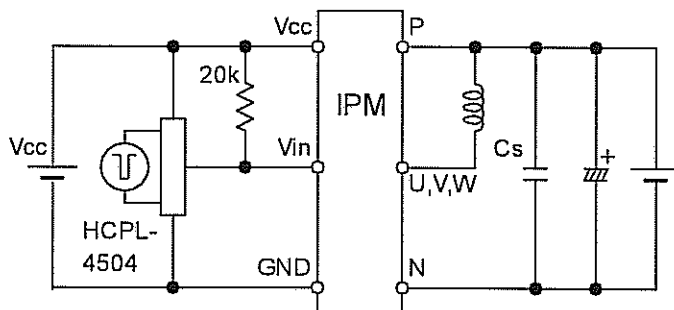


Figure6. Switching Characteristics Test Circuit

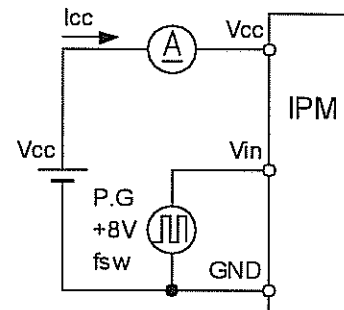


Figure7. Icc Test Circuit

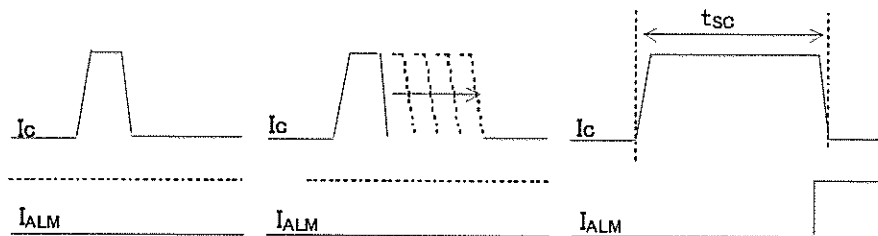


Figure8. Dification of tsc

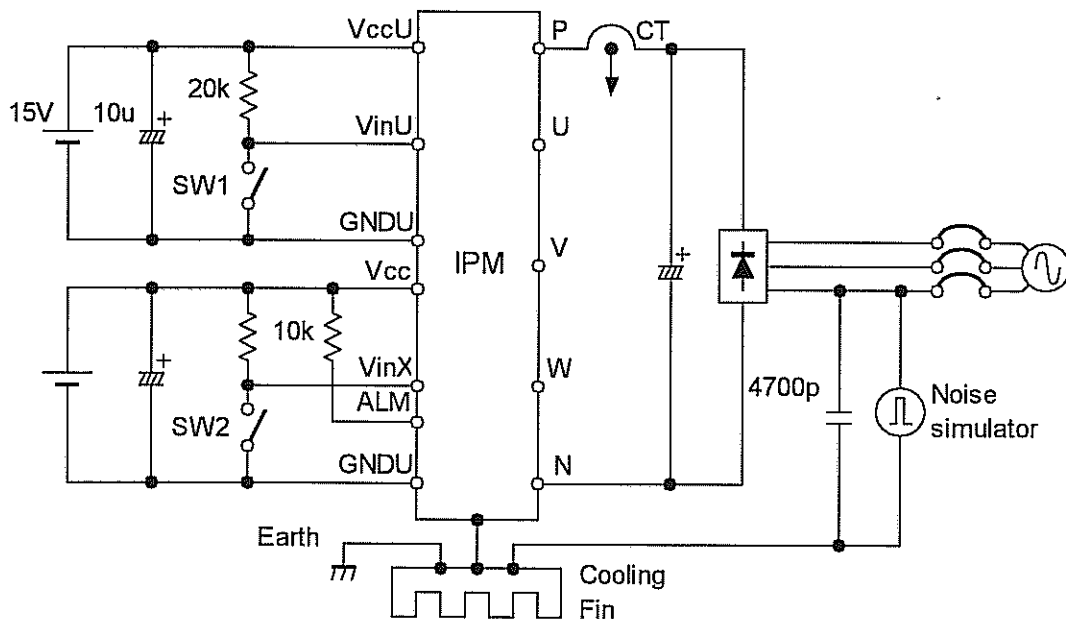


Figure9. Noise Test Circuit

10. Truth table

10.1 IGBT Control

The following table shows the IGBT ON/OFF status with respect to the input signal
The IGBT turn-on when Vin is at "Low" level under no alarm condition.

Input signal	Alarm output	Output (IGBT)
Low	High	On
Low	Low	Off
High	-	Off

10.2 Fault Detection

- (1) When a fault is detected at the high side, only the detected arm stops its output.
At that time the IPM doesn't any alarm.
- (2) When a fault is detected at the low side, all the lower arms stop their outputs
and the IPM outputs an alarm of the low side.

	Cause of fault	Operation of IGBT				Alarm Output
		U-phase	High side V-phase	W-phase	Low side	
High side U-phase	OC	OFF	*	*	*	High
	UV	OFF	*	*	*	High
	TJOH	OFF	*	*	*	High
High side V-phase	OC	*	OFF	*	*	High
	UV	*	OFF	*	*	High
	TJOH	*	OFF	*	*	High
High side W-phase	OC	*	*	OFF	*	High
	UV	*	*	OFF	*	High
	TJOH	*	*	OFF	*	High
Low side	OC	*	*	*	OFF	Low
	UV	*	*	*	OFF	Low
	TJOH	*	*	*	OFF	Low
	TcOH	*	*	*	OFF	Low

*: Depend on input logic.

11. Cautions for design and application

- (1) Trace routing layout should be designed with particular attention to least stray capacity between the primary and secondary sides of optical isolators by minimizing the wiring length between the optical isolators and the IPM input terminals as possible.

フォトカブラとIPMの入力端子間の配線は極力短くし、

フォトカブラの一次側と二次側の浮遊容量を小さくしたパターンレイアウトにしてください。

- (2) Mount a capacitor between Vcc and GND of each high-speed optical isolator as close to as possible.

高速フォトカブラのVcc-GND間に、コンデンサを出来るだけ近接して取り付けてください。

- (3) For the high-speed optical isolator, use high-CMR type one with $t_{pHL}, t_{pLH} \leq 0.8\mu s$.

高速フォトカブラは、 $t_{pHL}, t_{pLH} \leq 0.8\mu s$ 、高CMRタイプをご使用ください。

- (4) For the alarm output circuit, use low-speed type optical isolators with $CTR \geq 100\%$.

アラーム出力回路は、低速フォトカブラ $CTR \geq 100\%$ のタイプをご使用ください。

- (5) For the control power Vcc, use four power supplies isolated each. And they should be designed to reduce the voltage variations.

制御電源Vccは、絶縁された4電源を使用してください。また、電圧変動を抑えた設計として下さい。

- (6) Suppress surge voltages as possible by reducing the inductance between the DC bus P and N, and connecting some capacitors between the P and N terminals.

P-N間の直流母線は出来るだけ低インダクタンス化し、

P-N端子間にコンデンサを接続するなどしてサージ電圧を低減して下さい。

- (7) To prevent noise intrusion from the AC lines, connect a capacitor of some 4700pF between the three-phase lines each and the ground.

ACラインからのノイズ侵入を防ぐために、3相各線ーアース間に4700pF程のコンデンサを接続して下さい。

- (8) At the external circuit, never connect the control terminal GNDU to the main terminal U-phase, GNDV to V-phase, GNDW to W-phase, and GND to N-phase. Otherwise, malfunctions may be caused.

制御端子GNDUと主端子U相、制御端子GNDVと主端子V相、制御端子GNDWと主端子W相、

制御端子GNDと主端子Nを外部回路で接続しないで下さい。誤動作の原因になります。

- (9) Take note that an optical isolator's response to the primary input signal becomes slow if a capacitor is connected between the input terminal and GND.

入力端子-GND間にコンデンサを接続すると、フォトカブラ一次側入力信号に対する応答時間が

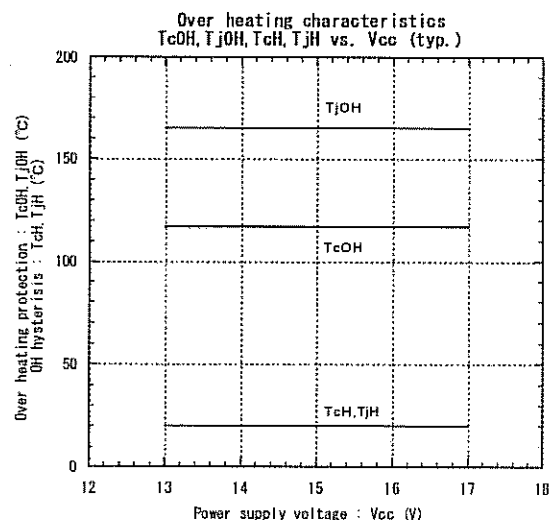
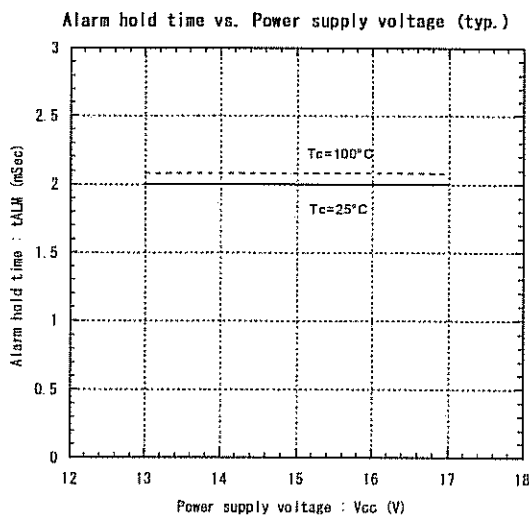
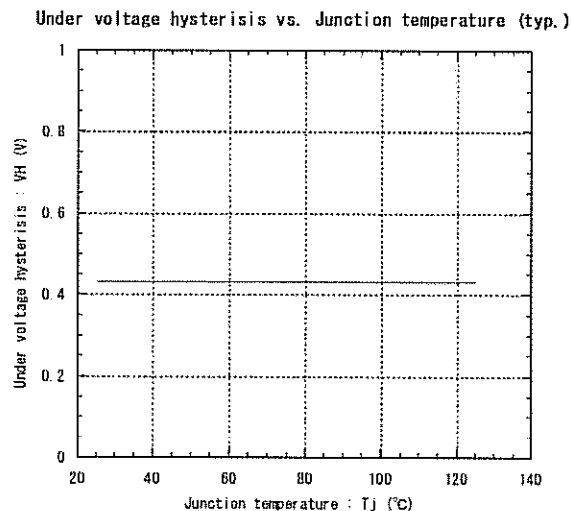
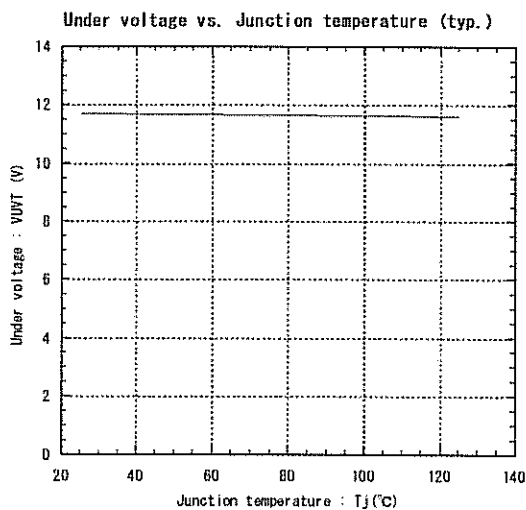
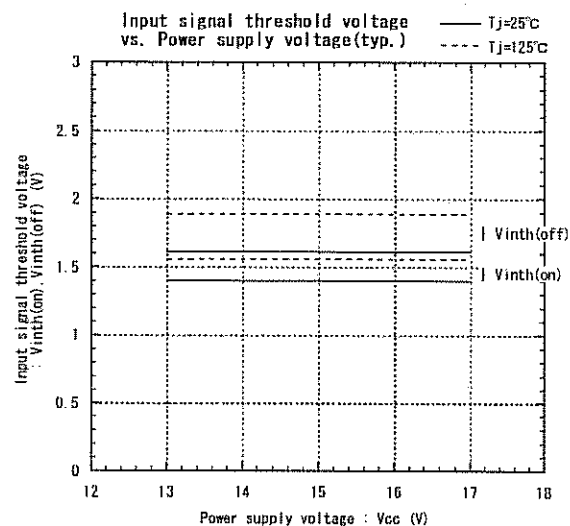
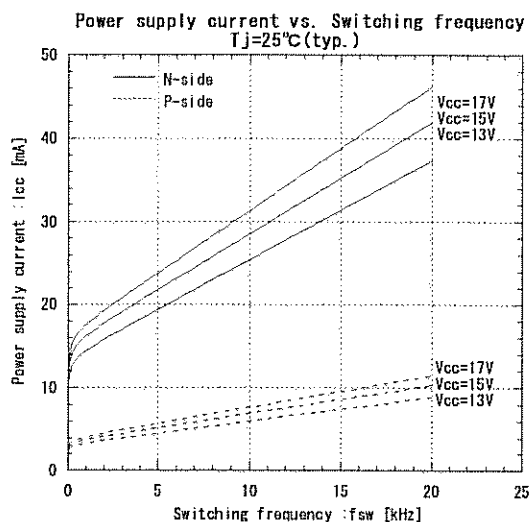
長くなりますのでご注意ください。

- (10) Taking the used isolator's CTR into account, design with a sufficient allowance to decide the primary forward current of the optical isolator.
 フォトカブラの一次側電流は、お使いのフォトカブラのCTRを考慮し十分に余裕をもった設計にしてください。
- (11) In case of mounting this product on cooling fin, use thermal compound to secure thermal conductivity. If the thermal compound amount was not enough or its applying method was not suitable, its spreading will not be enough, then, thermal conductivity will be worse and thermal run away destruction may occur.
 Confirm spreading state of the thermal compound when its applying to this product.
 (Spreading state of the thermal compound can be confirmed by removing this product after mounting.)
 素子を冷却フィンに取り付ける際には、熱伝導を確保するためのコンパウンド等をご使用ください。
 又、塗布量が不足したり、塗布方法が不適だったりと、コンパウンドが十分に素子全体に広がらず、
 放熱悪化による熱暴走破壊に繋がる事があります。コンパウンドを塗布する際には、
 製品全面にコンパウンドが広がっている事を確認してください。
 (実装した後に素子を取りはずすとコンパウンドの広がり具合を確認する事が出来ます。)
- (12) Use this product with keeping the cooling fin's flatness between screw holes within 100um at 100mm and the roughness within 10um. Also keep the tightening torque within the limits of this specification. Too large convex of cooling fin may cause isolation breakdown and this may lead to a critical accident. On the other hand, too large concave of cooling fin makes gap between this product and the fin bigger, then, thermal conductivity will be worse and over heat destruction may occur.
 冷却フィンはネジ取り付け位置間で平坦度を100mmで100um以下、表面の粗さは10um以下にしてください。
 過大な凸反りがあったりすると本製品が絶縁破壊を起こし、重大事故に発展する場合があります。
 また、過大な凹反りやゆがみ等があると、本製品と冷却フィンの間に空隙が生じて放熱が悪くなり、
 熱破壊に繋がる場合があります。
- (13) This product is designed on the assumption that it applies to an inverter use. Sufficient examination is required when applying to a converter use. Please contact Fuji Electric Co., Ltd if you would like to applying to converter use.
 本製品は、インバータ用途への適用を前提に設計されております。コンバータ用途へ適用される場合は、
 十分な検討が必要です。もし、コンバータへ適用される場合は御連絡ください。
- (14) Please see the 『IGBT-IPM APPLICATION MANUAL』 and 『IGBT MODULES APPLICATION MANUAL』.
 『IGBT-IPM アプリケーションマニュアル』及び『IGBTモジュール アプリケーションマニュアル』
 を御参照ください。

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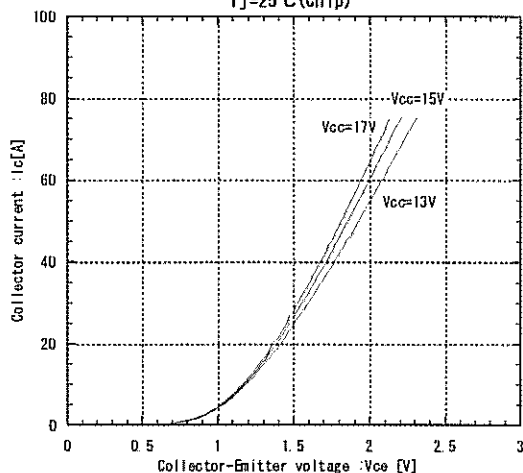
17. Characteristics

17.1 Control Circuit Characteristics (Representative)

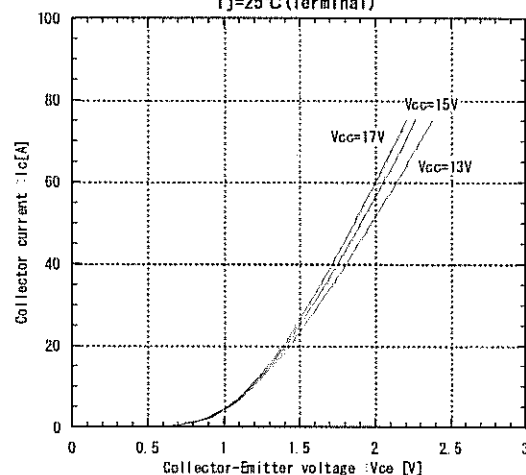


17.2 Main Circuit Characteristics (Representative)

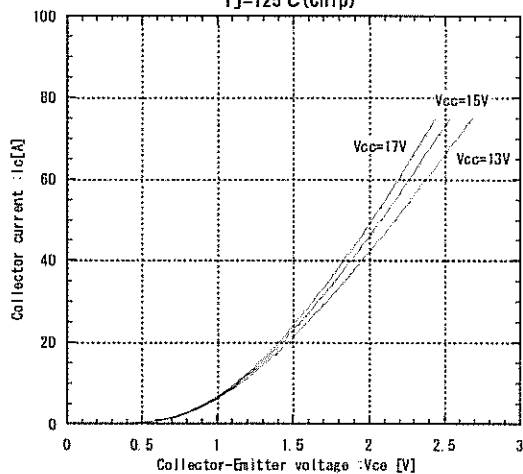
Collector current vs. Collector-Emitter voltage (typ.)
T_j=25°C (Chip)



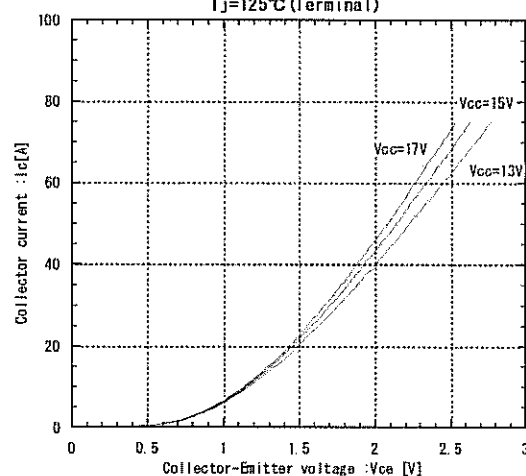
Collector current vs. Collector-Emitter voltage (typ.)
T_j=25°C (Terminal)



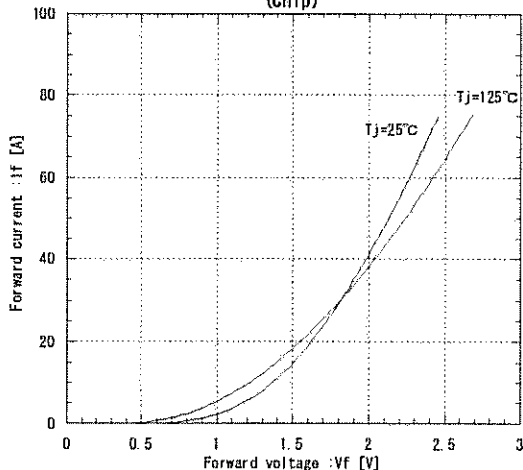
Collector current vs. Collector-Emitter voltage (typ.)
T_j=125°C (Chip)



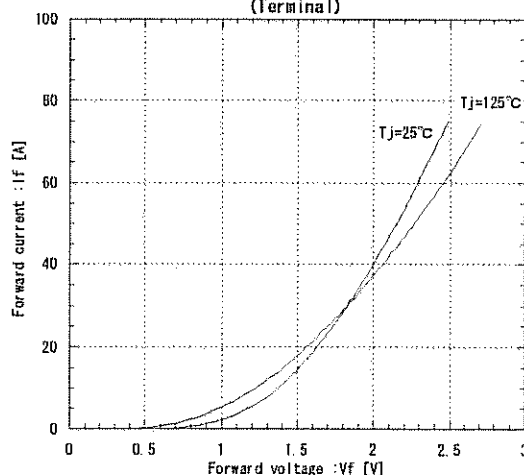
Collector current vs. Collector-Emitter voltage (typ.)
T_j=125°C (Terminal)



Forward current vs. Forward voltage (typ.)
(Chip)

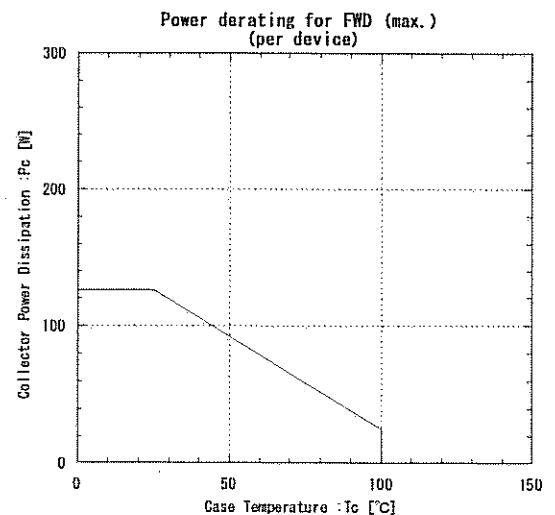
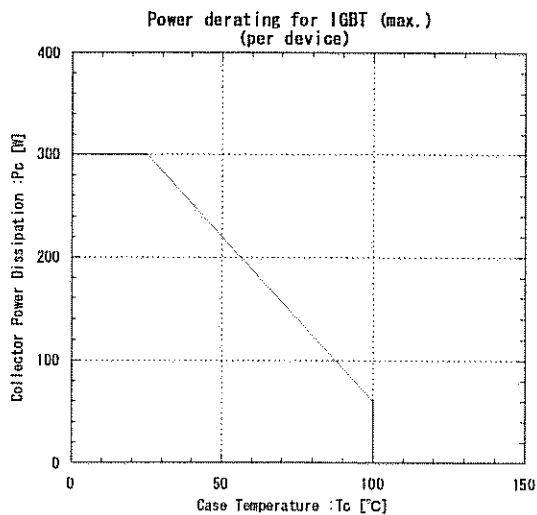
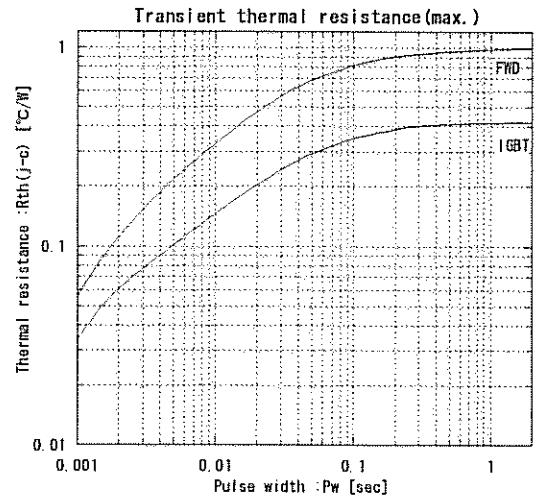
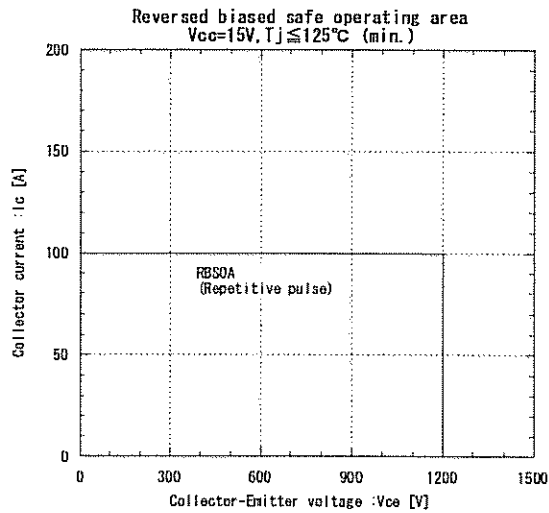
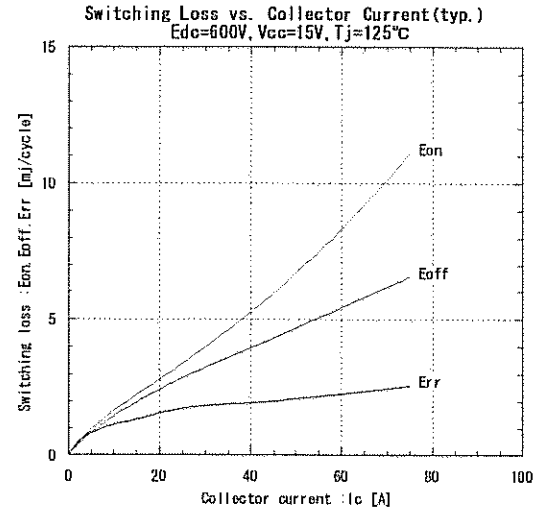
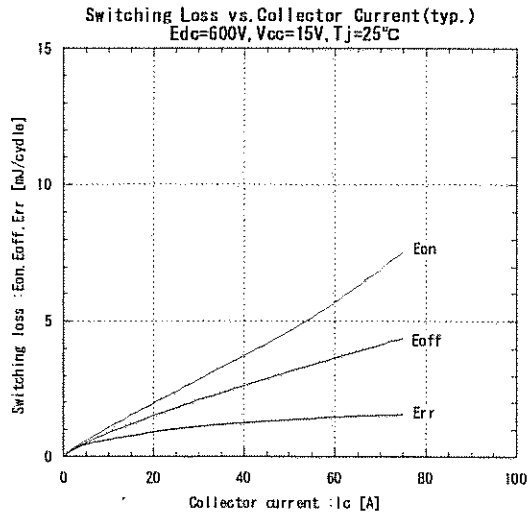


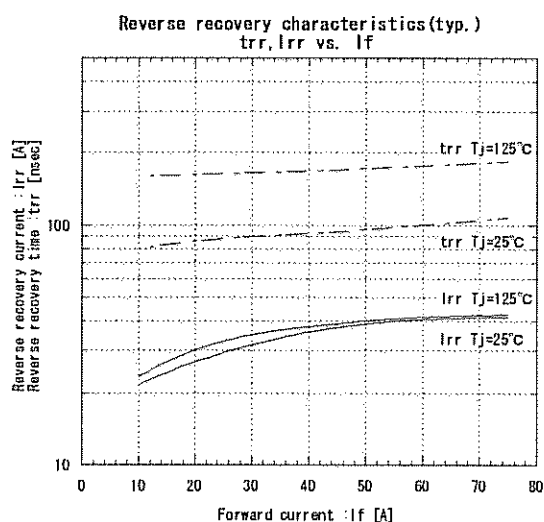
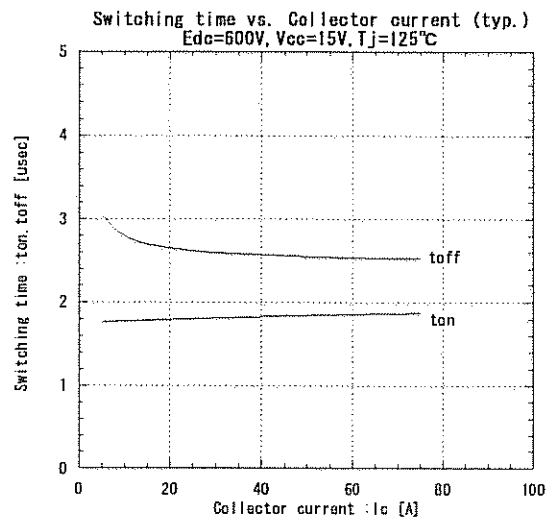
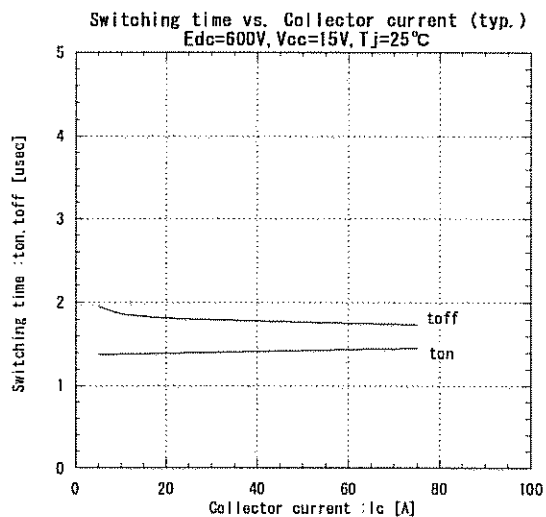
Forward current vs. Forward voltage (typ.)
(Terminal)



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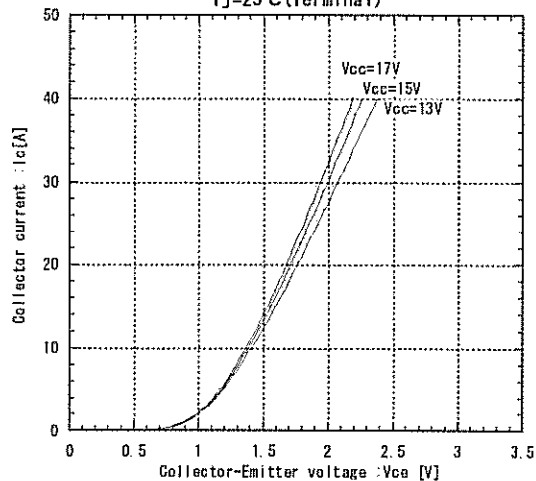
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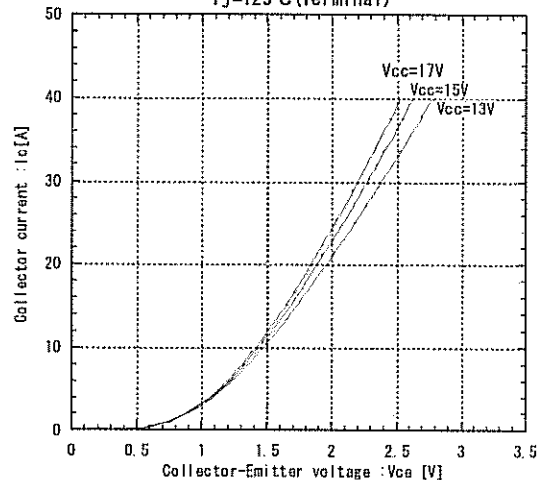


17.2 Dynamic Brake Characteristics (Representative)

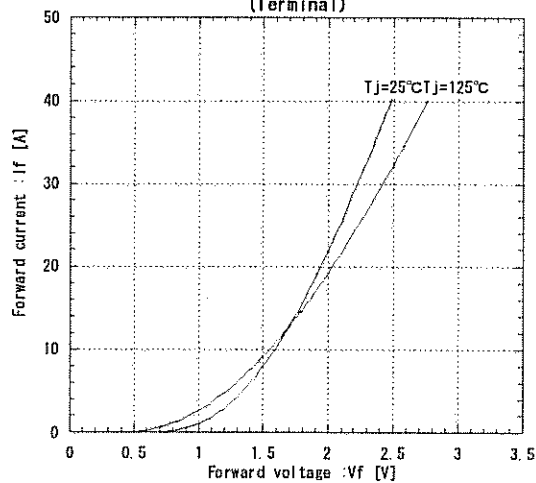
Collector current vs. Collector-Emitter voltage (typ.)
T_J=25°C (Terminal)



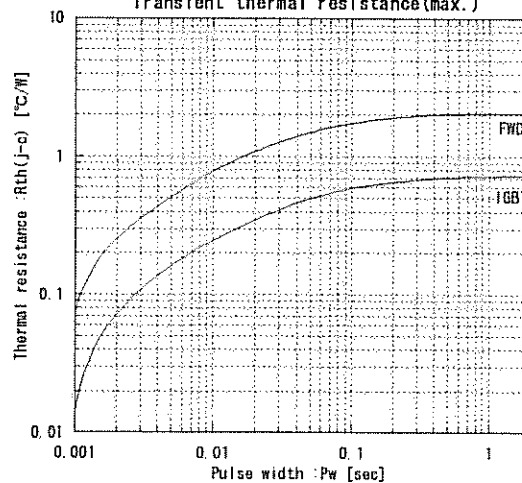
Collector current vs. Collector-Emitter voltage (typ.)
T_J=125°C (Terminal)



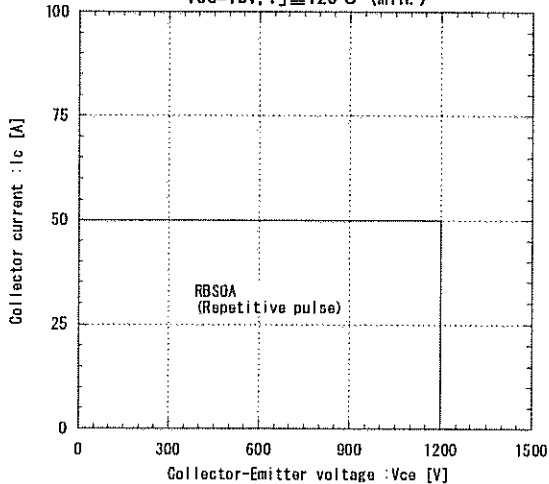
Forward current vs. Forward voltage (typ.)
(Terminal)



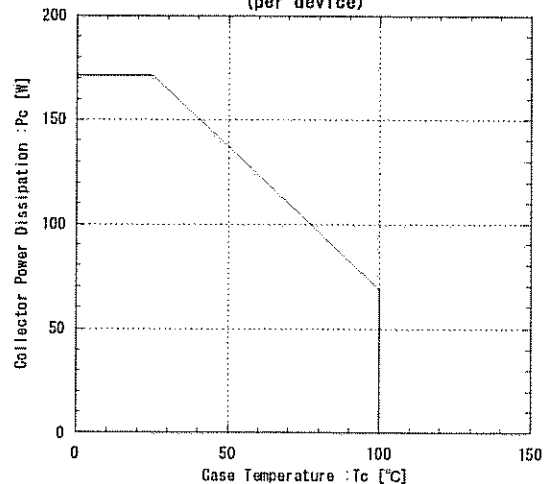
Transient thermal resistance (max.)



Reversed biased safe operating area
V_{ce}=15V, T_J≤125°C (min.)



Power derating for IGBT (max.)
(per device)



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18. Reliability Test

Test condions and results

Test cate- gories	No.	Test items	Test methods and conditions	Reference norms EIAJ ED-4701	Number of sample	Accept- ance number	Number of failure
Mechanical Tests	1	Terminal strength (Pull test)	Pull force : 40 N (main terminal) 10 N (control terminal) Test time : 10 ±1 sec.	Test Method 401 Method I	5	(1 : 0)	0
	2	Mounting Strength	Screw torque : 2.5 ~ 3.5 N·m (M5) Test time : 10 ±1 sec.	Test Method 402 method II	5	(1 : 0)	0
	3	Vibration	Range of frequency : 10~500 Hz Sweeping time : 15 min. Acceleration : 100 m/s ² Sweeping direction : Each X,Y,Z axis Test time : 6 hr. (2hr./direction)	Test Method 403 Condition code B	5	(1 : 0)	0
	4	Shock	Maximum acceleratic : 5000 m/s ² Pulse width : 1.0 ms Direction : Each X,Y,Z axis Test time : 3 times/direction	Test Method 404 Condition code B	5	(1 : 0)	0
	5	Solderability	Solder temp. : 235 ±5 °C Immersion duration : 5.0 ±0.5 sec. Test time : 1 time Each terminal should be Immersed in solder within 1~1.5mm from the body.	Test Method 303 Condition code A	5	(1 : 0)	0
	6	Resistance to soldering heat	Solder temp. : 260 ±5 °C Immersion time : 10 ±1sec. Test time : 1 time Each terminal should be Immersed in solder within 1~1.5mm from the body.	Test Method 302 Condition code A	5	(1 : 0)	0
Environment Tests	1	High temperature storage	Storage temp. : 125 ±5 °C Test duration : 1000 hr.	Test Method 201	5	(1 : 0)	0
	2	Low temperature storage	Storage temp. : -40 ±5 °C Test duration : 1000 hr.	Test Method 202	5	(1 : 0)	0
	3	Temperature humidity storage	Storage temp. : 85 ±2 °C Relative humidity : 85 ±5% Test duration : 1000hr.	Test Method 103 Test code C	5	(1 : 0)	0
	4	Unsaturated pressure cooker	Test temp. : 120 ±2 °C Atmospheric pressur : 1.7x10 ⁵ Pa Test humidity : 85 ±5% Test duration : 96 hr.	Test Method 103 Test code E	5	(1 : 0)	0
	5	Temperature cycle	Test temp. : Minimum storage temp. -40 ±5°C Maximum storage temp. 125 ±5°C Normal temp. 5 ~ 35°C Dwell time : Tmin ~ TN ~ Tmax ~ TN 1hr. 0.5hr. 1hr. 0.5hr. Number of cycles : 100 cycles	Test Method 105	5	(1 : 0)	0
	6	Thermal shock	Test temp. : High temp. side 100 ⁺⁰ °C Low temp. side 0 ⁺⁵ °C Fluid used : Pure water (running water) Dipping time : 5 min. par each temp. Transfer time : 10 sec. Number of cycles : 10 cycles	Test Method 307 method I Condition code A	5	(1 : 0)	0

Test categories	No.	Test items	Test methods and conditions	Reference norms EIAJ ED-4701	Number of sample	Acceptance number
Endurance Tests	1	High temperature reverse bias	Test temp. : $T_a = 125 \pm 5^\circ\text{C}$ ($T_j \leq 150^\circ\text{C}$) Bias Voltage : $V_C = 0.8 \times V_{CES}$ Bias Method : Applied DC voltage to C-E $V_{CC} = 15\text{V}$ Test duration : 1000 hr.	Test Method 101	5	(1 : 0)
	2	Intermittent operating life (Power cycle)	ON time : 2 sec. OFF time : 18 sec. Test temp. : $\Delta T_j = 100 \pm 5^\circ\text{deg}$ $T_j \leq 150^\circ\text{C}$, $T_a = 25 \pm 5^\circ\text{C}$ Number of cycles : 15000 cycles	Test Method 106	5	(1 : 0)

Failure Criteria

Item	Characteristic	Symbol	Failure criteria		Unit
			Lower limit	Upper limit	
Electrical characteristic	Leakage current	ICES	-	USL $\times$ 2.0	mA
	Saturation voltage	VCE(sat)	-	USL $\times$ 1.2	V
	Forward voltage	VF	-	USL $\times$ 1.2	V
	Thermal resistance	IGBT Rth(j-c)Q	-	USL $\times$ 1.2	$^\circ\text{C}/\text{W}$
		FWD Rth(j-c)D	-	USL $\times$ 1.2	$^\circ\text{C}/\text{W}$
	Over Current Protection	Ioc	LSL $\times$ 0.8	USL $\times$ 1.2	A
	Alarm signal hold time	tALM	LSL $\times$ 0.8	USL $\times$ 1.2	ms
	Over heating Protection	TcOH	LSL $\times$ 0.8	USL $\times$ 1.2	$^\circ\text{C}$
Visual inspection	Isolation voltage	Viso	Broken insulation		-
	Visual inspection [Peeling Plating and the others	-	The visual sample		-

LSL : Lower specified limit.
USL : Upper specified limit.

Note :

Each parameter measurement read-outs shall be made after stabilizing the components at room ambient for 2 hours minimum, 24 hours maximum after removal from the tests. And in case of the wetting tests, for example, moisture resistance tests, each component shall be made wipe or dry completely before the measurement.

Warnings

1. This product shall be used within its absolute maximum rating (voltage, current, and temperature).
This product may be broken in case of using beyond the ratings.
製品の絶対最大定格(電圧, 電流, 温度等)の範囲内で御使用下さい。
絶対最大定格を超えて使用すると、素子が破壊する場合があります。
2. Connect adequate fuse or protector of circuit between three-phase line and this product to prevent the equipment from causing secondary destruction.
万一の不慮の事故で素子が破壊した場合を考慮し、商用電源と本製品の間に適切な容量のヒューズ又はブレーカーを必ず付けて2次破壊を防いでください。
3. When studying the device at a normal turn-off action, make sure that working paths of the turn-off voltage and current are within the RBSOA specification.
通常のターンオフ動作における素子責務の検討の際には、
ターンオフ電圧・電流の動作軌跡がRBSOA仕様内にあることを確認して下さい。
4. Use this product after realizing enough working on environment and considering of product's reliability life. This product may be broken before target life of the system in case of using beyond the product's reliability life.
製品の使用環境を十分に把握し、製品の信頼性寿命が満足できるか検討の上、本製品を適用して下さい。
製品の信頼性寿命を超えて使用した場合、装置の目標寿命より前に素子が破壊する場合があります。
5. If the product had been used in the environment with acid, organic matter, and corrosive gas (For example : hydrogen sulfide, sulfurous acid gas), the product's performance and appearance can not be ensured easily.
酸・有機物・腐食性ガス(硫化水素, 亜硫酸ガス等)を含む環境下で使用された場合、
製品機能・外観などの保証は致しかねます。
6. Use this product within the power cycle curve (Technical Rep.No. : MT5F12959).
Power cycle capability is classified to delta-Tj mode which is stated as above and delta-Tc mode.
Delta-Tc mode is due to rise and down of case temperature (Tc), and depends on cooling design of equipment which use this product. In application which has such frequent rise and down of Tc, well consideration of product life time is necessary.
本製品は、パワーサイクル寿命カーブ以下で使用下さい(技術資料No.: MT5F12959)。
パワーサイクル耐量にはこの ΔT_j による場合の他に、 ΔT_c による場合があります。
これはケース温度(T_c)の上昇下降による熱ストレスであり、本製品をご使用する際の放熱設計に依存します。
ケース温度の上昇下降が頻繁に起こる場合は、製品寿命に十分留意してご使用下さい。
7. Never add mechanical stress to deform the main or control terminal.
The deformed terminal may cause poor contact problem.
主端子及び制御端子に応力を与えて変形させないで下さい。
端子の変形により、接触不良などを引き起こす場合があります。

8. According to the outline drawing, select proper length of screw for main terminal.

Longer screws may break the case.

本製品に使用する主端子用のネジの長さは、外形図に従い正しく選定下さい。

ネジが長いとケースが破損する場合があります。

9. If excessive static electricity is applied to the control terminals, the devices can be broken.

Implement some countermeasures against static electricity.

制御端子に過大な静電気が印加された場合、素子が破壊する場合があります。

取り扱い時は静電気対策を実施して下さい。

Caution

1. Fuji Electric Device Technology is constantly making every endeavor to improve the product quality and reliability. However, semiconductor products may rarely happen to fail or malfunction. To prevent accidents causing injury or death, damage to property like by fire, and other social damage resulted from a failure or malfunction of the Fuji Electric semiconductor products, take some measures to keep safety such as redundant design, spread-fire-preventive design, and malfunction-protective design.

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2. The application examples described in this specification only explain typical ones that used the Fuji Electric Device Technology products. This specification never ensure to enforce the industrial property and other rights, nor license the enforcement rights.

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3. The product described in this specification is not designed nor made for being applied to the equipment or systems used under life-threatening situations. When you consider applying the product of this specification to particular used, such as vehicle-mounted units, shipboard equipment, aerospace equipment, medical devices, atomic control systems and submarine relaying equipment or systems, please apply after confirmation of this product to be satisfied about system construction and required reliability.

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